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jc849 U.S. PTO
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PTO/SB/05 (4/98)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	00-088
First Inventor or Application Identifier	Feng Qian
Title	Viterbi Decoder With Adaptive Traceback
Express Mail Label No.	EL643644724US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231**

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [*Total Pages* 15] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 3]
4. Oath or Declaration [*Total Pages* 2]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [X] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. [ ] Other: ....

16. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: ______/______

Prior application information: Examiner ______ *Group / Art Unit:* ______

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

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Name (Print/Type)	Sandeep Jaggi	*Registration No. (Attorney/Agent)*	43,331
Signature	[signature]	*Date*	10-10-2000

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TOTAL AMOUNT OF PAYMENT ($) 690.00

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Feng Qian
Examiner Name	
Group / Art Unit	
Attorney Docket No.	00-088

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

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Deposit Account Name: LSI Logic Corporation

[X] Charge Any Additional Fee Required Under 37 CFR §§ 1.16 and 1.17

2. [ ] **Payment Enclosed:** [ ] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility filing fee	690
106	310	206	155	Design filing fee	
107	480	207	240	Plant filing fee	
108	690	208	345	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 690

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	6	-20** =		X		=	0
Independent Claims	1	- 3** =		X		=	0
Multiple Dependent					0	=	0

***or number previously paid, if greater; For Reissues, see below*

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim, if not paid
109	78	209	39	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	380	216	190	Extension for reply within second month	
117	870	217	435	Extension for reply within third month	
118	1,360	218	680	Extension for reply within fourth month	
128	1,850	228	925	Extension for reply within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,210	241	605	Petition to revive - unintentional	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	690	246	345	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	690	249	345	For each additional invention to be examined (37 CFR § 1.129(b))	
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Other fee (specify) ______					

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SUBTOTAL (3) ($) 0

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	Sandeep Jaggi	Registration No. (Attorney/Agent)	43,331	Telephone	408/954-4923
Signature	[signature]			Date	10-10-2000

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Feng Qian

For : Viterbi Decoder With Adaptive Trace-Back

Atty Docket : 00-088

I hereby certify that this correspondence is being deposited with the U S Postal Service as Express Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington D.C. 20231, on the date indicated below:

Manu Kashyap

Date 10/10/00 Signature

Jc926 U.S. PTO 09/686675 10/11/00

TRANSMITTAL LETTER FOR PATENT APPLICATION

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir,

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1. Fee Transmittal Form (in duplicate).
2. Patent Application comprising the following :

    a. Specification, pages = 15

    b. Drawing, sheets = 3

    c. Assignment and declaration with power of attorney.

It is respectfully requested that the Commissioner accord the enclosed patent application a filing date and a serial number.

If it is determined that any additional fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 12-2252.

LSI Logic Corporation
1551 McCarthy Blvd., MS D-106
Milpitas, CA 95035
408/433-7475

Date: 10/10/00

Respectfully submitted,

Sandeep Jaggi

Reg. No. 43,331

PATENT

Docket: 00-088

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Manu Kashyap
[NAME OF PARALEGAL]

Viterbi Decoder With Adaptive Traceback

By:

Feng Qian
25851 Majorca Way
Mission Viejo, CA92692
Citizenship: USA
949-582-2826

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a method and apparatus for decoding convolutionally encoded signals. Such signals are commonly used in communications and recording systems that employ error correction to combat signal corruption.

Description of the Related Art

One increasingly popular redundant coding scheme used in wireless and other types of communications systems is convolutional coding, in which the coding of particular symbol depends upon the value of that symbol and the value of a certain number of symbols preceding and succeeding that particular symbol.

It would be desirable to improve upon conventional maximum likelihood sequence estimation ("MLSE") decoders such as Viterbi decoders, which are commonly used to decode convolutionally encoded data. If $\underline{s}_k$ is a vector that represents an actual transmitted sequence of symbols and $\underline{r}$ is a vector that represents the actual signals received by a mobile, a Viterbi decoder effectively tests all of the possible values of $\underline{s}_k$ and selects the $\underline{\hat{s}}$ that maximizes the summation ("cross correlation") $\sum_n c[n]r[n]\, s_k[n] = \underline{s}_k^T C \underline{r}$ where c[n] defines the channel gain for a transmitted symbol for sample n (and thus C is a diagonal matrix with these values). (The $\underline{s}_k$ that maximizes

the cross correlation is the $\underline{s}_k$ that minimizes the "distance" between $\underline{r}$ and $\underline{s}_k$.) For more details regarding Viterbi decoders, see, for example, "Digital Communications", John G. Proakis (3d edition 1995).

The best $\underline{s}_k$ may be represented as a path through nodes in a diagram (known as a trellis), where lines ("transitions") between nodes in adjacent time steps represent whether an input symbol (information bit) was a 0 or a 1 (for binary coding). The nodes ("states") in vertical columns represent the values of prior input symbols. A "path" through the trellis therefore represents a particular sequence of input symbols. Figure 1 shows an example of a trellis with only two paths shown. The time steps indicate a decoder trellis beginning at time t=0 to time t=4. At each time step, the decision units of the decoder contain the value of the cross correlation of the most likely path to the state of interest. Thus, the decoder trellis contains multiple paths from an initial state to a given state several time steps later.

However, only one path has the highest cross correlation and is the most likely path. The most likely path to a particular state within a given time step is found by starting at that particular state at that given time step and tracing backward (a "traceback") along the chosen transitions. Information bits that correspond to the transitions along the path are the decoded data. An information bit equal to 0 is shown is a solid line; an information bit equal to 1 is shown as a dotted line. Thus, the path shown in Figure 1 ending at state A at time t=0 corresponds to an information bit sequence equal to 0100.

A weight is computed for each state at each time, where the weight for a particular state at a particular time corresponds to the likelihood that the encoder was in that state at that time. The weight is equal to the weight of a previous state that transitioned to the current state plus a weight based upon the likelihood of the transition. For example, node 10 at time t=4 has a metric of four which equals the weight of node 12 at time t=3 plus the weight for the transition between those nodes. The node at any given time with the highest weight is the node that ends the most likely path and is therefore the node from which the traceback will occur.

To achieve good noise performance from the decoding process, the traceback length must generally be several times the constraint length (the number of input bits upon which an output depends; this is the length of a shift register that may be used to perform the encoding) of the code. In current code division multiple access ("CDMA"), a traceback length L = 5*K, where K is the constraint length, is frequently taken as the minimum acceptable traceback length.

For a decoder with M bits of memory, M-L valid bits can be obtained after each traceback. If an incoming data frame consists of N information bits (assumed to be greater than M), the number of L bit tracebacks is (N-K)/(M-L), which corresponds to a computation requirement of M*(N-K)/(M-L), where a computation is assumed to be a one bit traceback. (The one bit traceback is used simply as a "yardstick.") If M=L+1, this equation reduces

to (L+1)*(N-K), which corresponds to the smallest memory and the greatest computational overhead.

Instead of performing periodic, partial tracebacks, if the decoder memory is sufficiently large, an entire incoming data frame may be stored and a full traceback of length (N-K) performed. Thus the full traceback is less computationally intensive than the periodic traceback scheme by a factor of M/(M-L). However, larger memories (greater M) are costly.

It would be desirable to implement the partial traceback scheme, with its smaller memory requirement, while at the same time decreasing its computational overhead.

SUMMARY OF THE PRESENT INVENTION

These and other needs are met by the present invention, which provides a method and apparatus for decoding transmitted data that has been generated by encoding information data with a convolutional encoder that generates convolutional codes based on an input sequence of data, where the encoder has a constraint length K and a rate k/n.

According to an embodiment of the present invention, L-1 data bits of a traceback beginning at a time step T are stored, where L is the traceback length; these L-1 data bits are the data bits corresponding to the L-1 time steps backwards from time step T. The maximum likelihood encoder state for time T is also saved. (The L-th data bit is the desired data bit as in conventional convolutional decoders.) In a subsequent partial traceback, preferably beginning at time T+1 that ends at time step T, the maximum likelihood encoder state for time T determined from the partial traceback is compared with the stored encoder state for time T. If they correspond to the same encoder state, the L-1 stored data bits are designated as the last L-1 data bits of the current (partial) traceback.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

Figure 1 is an example of a trellis diagram.

Figure 2 represents a digital communications system, in which a convolutional decoder including the present invention may be used.

Figure 3 is a flow chart that shows the operation of a possible embodiment of a convolutional decider constructed according to the teachings of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The MLSE decoder that is described is a Viterbi decoder but the invention may be applied to any type of MLSE decoder.

General System Description

Figure 2 represents a digital communications system 140 comprising a discrete-time channel 142 interposed between an encoder 144 and a decoder 130. Discrete-time channel 142 comprises a modulator 146, a channel 148 and a demodulator 150. An interleaver 145 is interposed between the encoder 144 and the modulator 146. A deinterleaver 151 is interposed between the decoder 130 and the demodulator 150. Channel 148 may be a transmission channel or a storage medium being written to and read from. Interleaver 145 receives a digital output signal from encoder 144 and interleaves this digital output signal over a certain time period, which is usually predetermined and known as a frame. Modulator 146 serves to translate the digital output signal from interleaver 145 into signals suitable for channel 148 and thereafter drives the signals across channel 148.

Channel 148 may suffer from interference that corrupts said signals, the interference possibly taking form in any combination of additive noise, cross channel interference, multi-path interference, and channel fading. Demodulator 150 serves to receive the signals from channel 148 while minimizing the interference as much as is practical, and thereafter translate the signals into digital signals for input to deinterleaver 151, which

deinterleaves the digital signal and provides it to decoder 130. Discrete-time channel 142 can thus be viewed as a unit accepting digital input signals and producing possibly corrupted digital output signals although the present invention is not limited to noisy channels.

The decoder 130 has a memory 131.

Encoder 144 is a convolutional encoder which serves to add redundancy to input data signal 152. In particular, the encoder 144 comprises a shift register coupled to various arithmetic units (such as modulo 2 adders) that form n bits of output based on the bits in the shift register. For a simple shift register, where each shift of the register causes one bit to be shifted in and out of the register (i.e. each data bit is shifted to the next location in the register) each input bit corresponds to n bits of encoder 144 output and 1/n is known as the rate of the encoder 144. If the shift register has K elements, the K-1 most recent bits input into the encoder correspond to a state. K is known as the constraint length. For binary input data, there are therefore 2^{K-1} possible encoder states.

The added redundancy (n bits per information bit) allows for detection and correction of errors that may result from corruption of signals passing across discrete-time channel 142. The error detection and correction is performed by decoder 130.

Flow Chart of Operation

Figure 3 is a flow chart that details the traceback operation of the decoder 130. At block 200, the decoder 130 receives input data to be decoded. At block 210, the decoder 130 computes the current branch metric. This block is known in the art will not be further discussed. At block 220, the decoder 130 selects the surviving state. This block is well known in the art and will not be further discussed. At block 230, the decoder 130 checks whether L+K decoding cycles (i.e. one decoding cycle per time step) have occurred, where L is the traceback length and K is the constraint length. If not, control passes back to block 210. If so, control passes to block 240, where the decoder 130 stores the starting state of the traceback in the memory 131 (e.g., with reference to Figure 1, the state A at time t=4).

At block 250, the encoder determines whether the traceback to be performed is the first traceback of the current data frame. If so, control passes to block 260, where a full traceback is performed. For each time step transition within the traceback, the data bit corresponding to the transition between the current state (e.g. the encoder state at time step t=4) and the next most recent state (e.g. the state at time step t=3) is stored in the memory 131. Control passes back to block 210. Otherwise, if at least one traceback has already occurred for the data frame, control passes to block 270.

In block 270, the decoder 130 performs a partial traceback; in the preferred embodiment, the partial traceback traces back one time step. Control passes to block 280, which compares the finishing state of the partial

traceback (e.g. the state at time step t=4 for a traceback beginning at time t=5) to the initial state of the most previous traceback (e.g. the traceback that began at time step t=4). If these quantities are not equal, control passes back to block 260, and a "normal" traceback is performed (beginning from the end of the partial traceback).

If these quantities are equal, control passes to block 290, where the L-1 bits stored from the previous traceback are designated as the L-1 final bits of the current traceback. In other words, the current traceback bits are taken to be the concatenation of (a) the bit corresponding to the first encoder transition of the current traceback; with (b) the L-1 final bits of the previous traceback. The last bit stored from the previous traceback (i.e. the bit corresponding to the transition from the third to last encoder state to the second to last encoder state of the previous traceback) is designated as the desired data bit for the traceback. (The transition from the third to last state to the second to last state of the previous traceback corresponds to the transition from the second to last state to the last state of the current traceback.)

Conclusion

Numerous variations and modifications will become apparent to those skilled in the art once the above disclosure is fully appreciated. It is intended that the following claims be interpreted to embrace all such variations and modifications.

WHAT IS CLAIMED IS:

1. A method for decoding transmitted data that has been generated by encoding a sequence of information data with a convolutional encoder that generates convolutional codes based on an input sequence of information data, the encoder characterized by a constraint length K and a rate k/n, the method employing a decoder with a memory, the method comprising the steps of:

(a) storing a first encoder state corresponding to a first time step;

(b) beginning at the first time step, performing a first traceback through a plurality time steps, thereby determining a first input bit corresponding to an encoder state transition from the last time step of the first traceback to the second to last time step of the first traceback;

(c) storing in the decoder memory a first possible input bit corresponding to a transition from an encoder state at a third time step within the first traceback, to an encoder state at a fourth time step within the first traceback, where neither the third nor fourth time steps are the last time step;

(d) performing a second traceback beginning at a second time step and encompassing the first time step, thereby determining a second encoder state at the first time step;

(e) comparing the first encoder state with the second encoder state;

(f) if the first encoder state is equal to the second encoder state, designating the first possible input data bit as a decoded data bit corresponding to a transition from the encoder state at the third time step to the encoder state at the fourth time step.

2. The method of claim 1 wherein the second time step is the next time step after the first time step.

3. The method of claim 1 wherein the third time step is the next time step after the last time step.

4. The method of claim 1 wherein the second traceback ends at the first time step.

5. The method of claim 1 wherein the second traceback traces back through one time step.

6. The method of claim 1 further comprising the steps of storing in the decoder memory, for each transition within the first traceback, a possible

input bit corresponding to the transition, thereby storing a plurality of possible input data bits in addition to the first possible input bit.

ABSTRACT OF THE DISCLOSURE

In a convolutional decoder using partial traceback, L-1 data bits of a traceback beginning at a time step T are stored, where L is the traceback length; these L-1 data bits are the data bits corresponding to the L-1 time steps backwards from time step T. The maximum likelihood encoder state for time T is also saved. (The L-th data bit is the desired data bit as in conventional convolutional decoders.) In a subsequent partial traceback, preferably beginning at time T+1 that ends at time step T, the maximum likelihood encoder state for time T determined from the partial traceback is compared with the stored encoder state for time T. If they correspond to the same encoder state, , the L-1 stored data bits are designated as the last L-1 data bits of the current (partial) traceback.

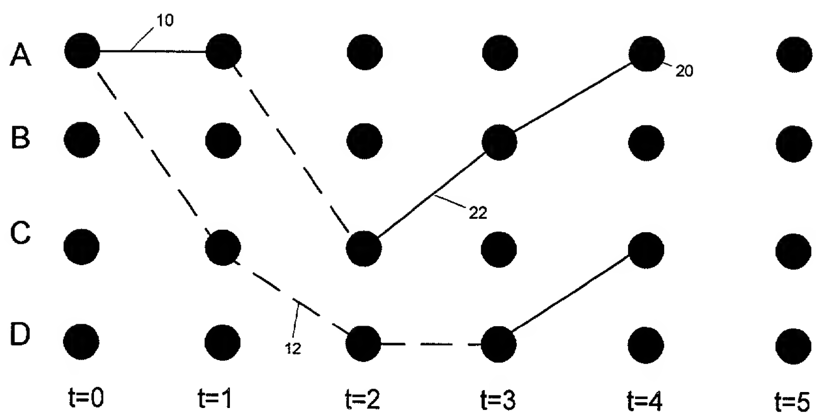

Figure 1

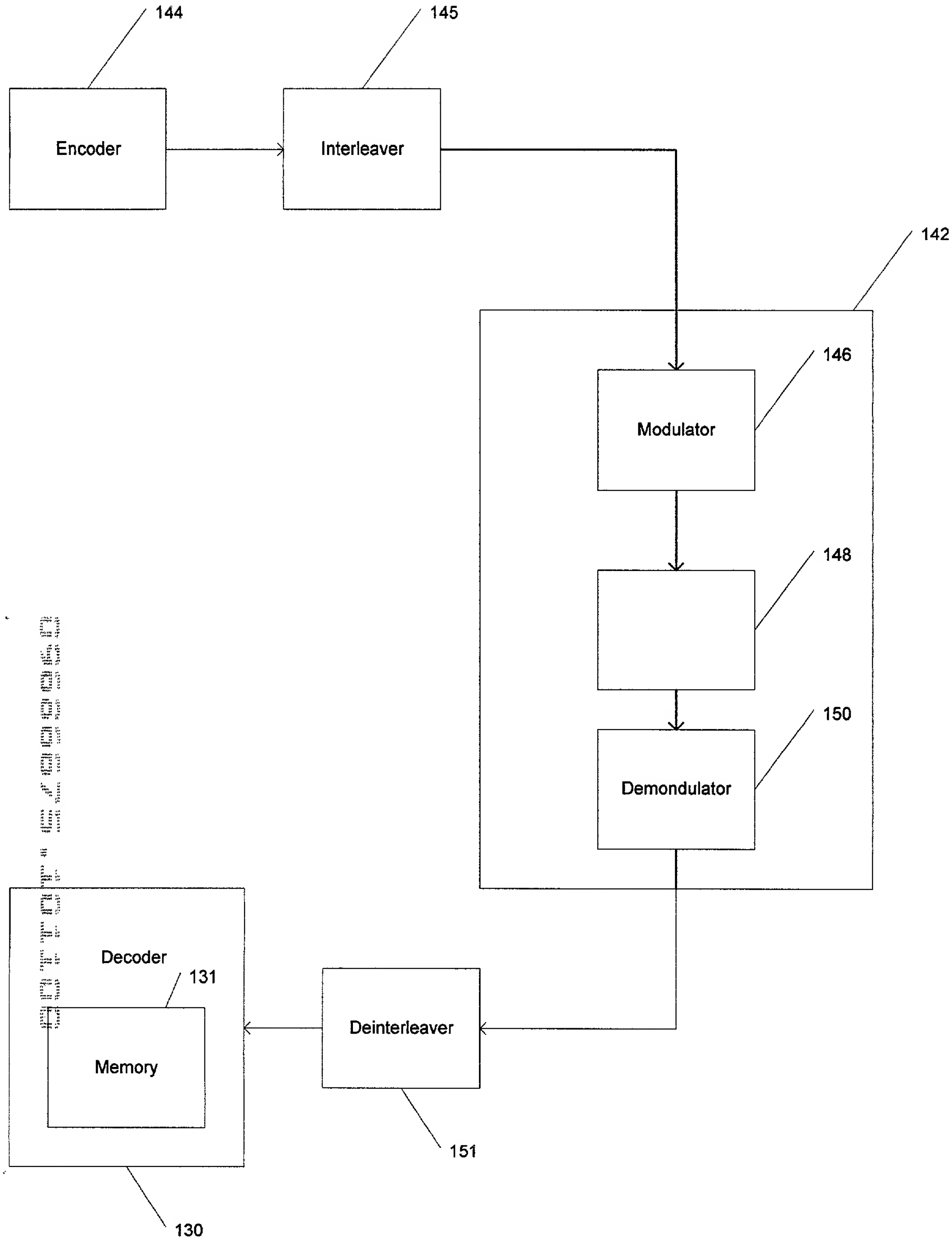
144
145
Encoder
Interleaver
142
146
Modulator
148
150
Demondulator
Decoder
131
Memory
Deinterleaver
151
130

Figure 2

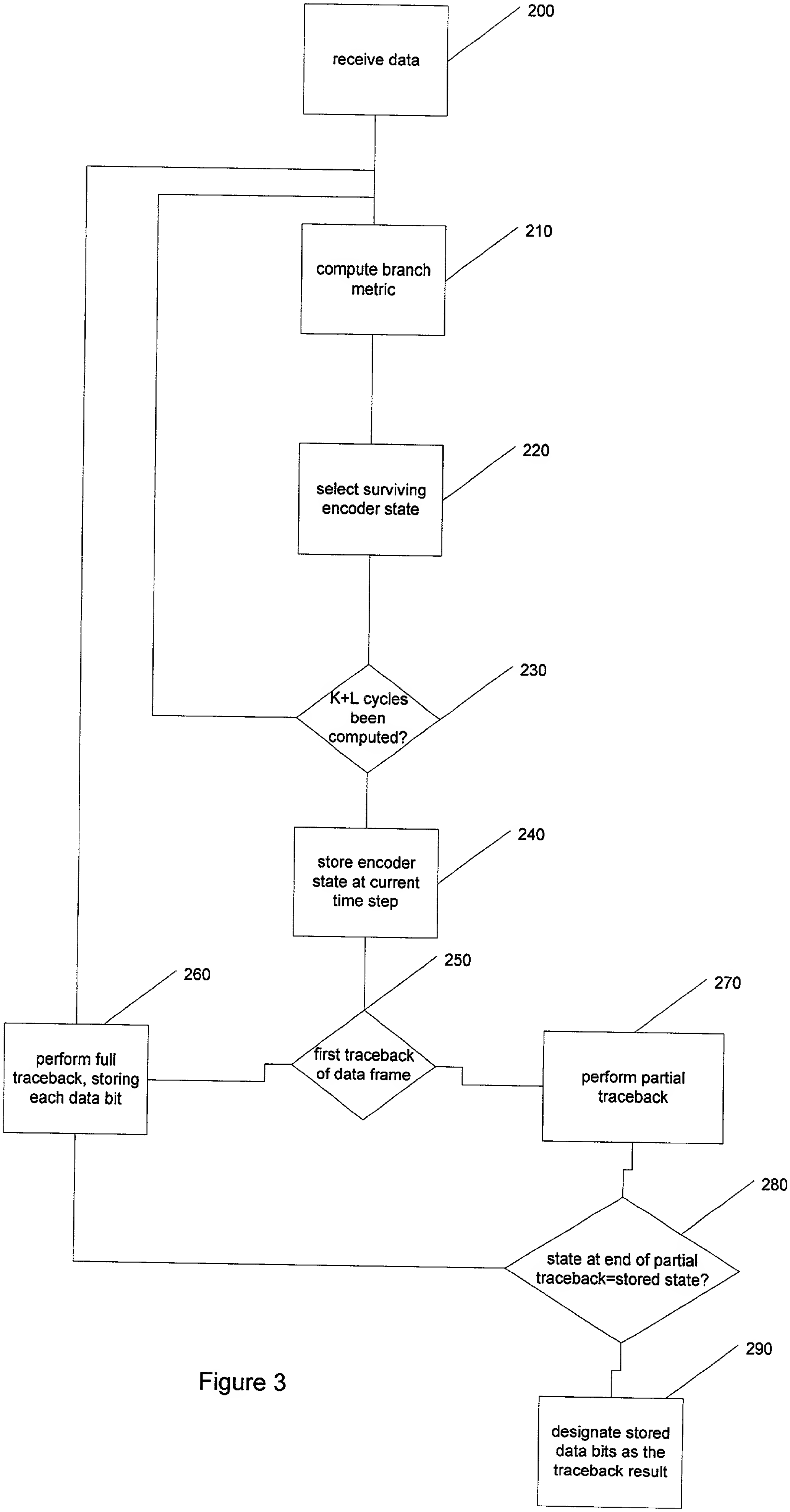
receive data
200
compute branch metric
210
select surviving encoder state
220
K+L cycles been computed?
230
store encoder state at current time step
240
first traceback of data frame
250
perform full traceback, storing each data bit
260
perform partial traceback
270
state at end of partial traceback=stored state?
280
designate stored data bits as the traceback result
290

Figure 3

Declaration, Power of Attorney, Correspondence Address, and Petition

Docket Number : **00-088**

Declaration

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first, and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Viterbi Decoder With Adaptive Trace-Back

the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Power of Attorney

I hereby appoint David G. Pursel, Reg. 28,659; Ralph R. Veseli, Reg. 33,807; Bruce R. Hopenfeld, Reg. 39,714; Gary Edward Ross, Reg. 29,431; Lloyd E. Dakin, Reg. 38,423; and Sandeep Jaggi, Reg. 43,331; as my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected therewith and before competent international authorities.

Correspondence Address

Please send all correspondence to:

LSI Logic Corporation
Corporate Legal Department
Intellectual Property Services Group
1551 McCarthy Blvd., M/S D-106
Milpitas, CA 95035
Phone: (408) 433-8708
Fax: (408) 433-7770

Petition

Wherefore I pray that Letters Patent be granted to me for the invention or discovery described and claimed in the foregoing specification and claims, and I hereby subscribe my name to the foregoing specification and claims, declaration, power of attorney, and this petition.

Declaration, Power of Attorney, Correspondence Address, and Petition

First named inventor

First Name Feng **Last Name:** Qian

Inventor's Signature: _______________ **Date** 8/14/2000

Address 25851 Majorca Way

City Mission Viejo CA 92692 United States

Citizenship United States